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Review
The chemical polishing of semiconductors

BRIAN TUCK
Department of Electrical and Electronic Engineering, The University of Nottingham, UK

The review first considers the types of reaction which occur when a semiconductor is chemically polished, taking the dissolution of silicon in nitric acid solutions as an example. Most initial reactions are of the oxidation-reduction type, which can be separated into their anodic and cathodic components. It is shown that electrons and holes can take part in both parts of the reaction, so chemical polishing can interfere with the carrier concentrations close to the surface being polished. In general, the products of the initial reaction are not soluble, so it is necessary to include a component in the polishing solution which will react to give soluble material, which can then be removed from the surface. The factors controlling the dissolution rate are then outlined. It is shown that polishing processes are conveniently divided into two main groups: (1) those for which the rate-limiting process is some aspect of the chemical reaction, and (2) those for which diffusion of atoms to or from the surface controls the rate.

Crystallographic effects are discussed. It is shown that different surface orientations are etched at different rates, and possible reasons for this are outlined. The various types of surface features that can be observed under the microscope after polishing are then described, and their origins are discussed. A review of some of the more extensive investigations is then given, followed by an Appendix containing lists of chemical polishes that have been used for semiconductors of groups IV, III-V and II-VI.

1. Introduction

Chemical polishing is one of the most commonly used techniques in semiconductor work. In almost every fabrication process using a semiconductor slice or, indeed, any experiment involving a semiconductor, it is necessary at some point to immerse the slice in a liquid in order to remove material. The great bulk of polishing work is carried out, therefore, not by workers studying the subject, but as part of some other process, such as device manufacture. Suitable etches are often found on a trial and error basis, and chemical polishing is often considered an art rather than a science. A good deal of research has been done in this field, however, and this review attempts to outline the elements of the subject in a manner which will be understood by the wide range of materials scientists who use semiconductor polishing techniques.

There are several reasons why a semiconductor might be polished, the most common being: (1) to remove the layer of material close to the surface that has been damaged by mechanical cutting or abrading, (2) to produce a shiny, flat surface, and (3) to study the defect structure of the semiconductor. Certain chemical polishes have the effect of producing surface features on the semiconductor which can be related to the defects in the crystal. This is especially true of dislocations, which often form etch pits at their points of intersection with a surface, thus providing a simple way of estimating dislocation densities.

This review first considers the types of chemical reaction involved in polishing and then goes on to describe the dissolution kinetics. Surface features are then discussed and a brief account is given of some of the more important investigations. A list of polishes that have been used for semiconductors of groups IV, III-V and II-VI is given in the Appendix. It is worth noting that the words "polishing" and "etching" are used here simply to mean the removal of material by dissolution.

2. The chemical reaction

2.1. Oxidation-reduction processes

In almost all semiconductor polishing processes the basic initial reaction is one in which the material is oxidized. In general the surface atoms will not pass into solution in this state and it is necessary to have another component in the etch which will react with the oxidized semiconductor to form a soluble complex. Polishing solutions, therefore, contain an oxidizing agent, of which the most commonly used are HNO_3, H_2O_2 and bromine, and also a complexing agent such as HF. Many solutions also contain a constituent which simply dilutes the solution. This is often water, and it must also be remembered that many chemicals contain a high proportion of water in the form in which they are usually used.

It follows from the above that more than one chemical reaction is involved in a typical polishing process, so the situation is far from simple. In fact, further factors often arise which complicate matters still more. Some of the constituents might fulfill more than one of the above functions, for instance. Reactions might also take place between the constituents, independently of the semiconductor: the action of an etch consisting of HNO_3 and HCl (aqua regia), for instance, has been attributed to a reaction of the acids, producing chlorine [1]

$$HNO_3 + 3HCl = NOCl + 2H_2O + Cl_2 .$$

Put in general terms, the oxidation of an atom involves its becoming more positively charged. The negative charge which it loses is taken up by the oxidizing agent, which itself is reduced. Consider a solid, M, dissolving in some oxidizing liquid. The first stage is for an atom at the surface to become a positive ion (assumed singly-charged here, for the sake of simplicity):

$$M \rightarrow M^+ + e^- . \qquad (1)$$

This is called the anode reaction and gives rise to a "spare" electron in the solid. The electron is taken up by the oxidizing agent, X, which diffuses through the liquid to the surface of the solid:

$$X + e^- \rightarrow X^- . \qquad (2)$$

This is called the cathode reaction. Note that dissolution takes place only at the anode. In a simple process, anode and cathode areas are finely distributed over the surface and any one area acts as anode and cathode alternately. Equations 1 and 2 can be combined to give the overall reaction that is taking place:

$$M + X \rightleftharpoons MX . \qquad (3)$$

If the reaction product is soluble, then an atom has been removed; if it is not soluble, then a complexing agent is required and a further reaction must take place.

As an example of this type of process, let us consider the dissolution of silicon in an etch composed of HNO_3, HF and H_2O. In this system, HNO_3 acts as the oxidizing agent, HF produces the soluble product and water is a diluent. The following mechanism is believed to operate over most compositions of the etching solution. The anodic reaction starts with the production of silicon ions:

$$Si \rightarrow Si^{4+} + 4e^- . \qquad (4)$$

The ion can react with water in the system to give silicon oxide:

$$Si^{4+} + 2H_2O \rightarrow SiO_2 + 4H^+ . \qquad (5)$$

The four negative charges left behind in the silicon are used up in the cathode reaction. It is generally agreed that the steady-state reaction takes place in several stages, i.e. the negative charges are not directly taken up by the nitric acid, but by products of the acid which are stronger oxidizing agents. An initial reaction takes place between nitric and nitrous acids:

$$HNO_2 + HNO_3 \rightleftharpoons 2NO_2 + H_2O . \qquad (6)$$

The charges are then taken up by the NO_2:

$$2NO + 2e^- \rightleftharpoons 2NO_2^- . \qquad (7)$$

The negative ions then react again to give more nitrous acid which feeds back to Equation 6:

$$2NO_2^- + 2H^+ = 2HNO_2 . \qquad (8)$$

The overall cathode reaction is, therefore:

$$HNO_2^- + 2H^+ + 2e^- = HNO_2 + H_2O \qquad (9)$$

and adding together the anode and cathode reactions gives the equation for the whole process as:

$$Si + 2HNO_3 = SiO_2 + 2HNO_2 . \qquad (10)$$

The question now arises of where the nitrous acid comes from in the first place to power Equation 6. The answer must be that Equations 6 to 10 refer only to the steady state. In this condition, more than enough HNO_2 is provided by Equation 8, i.e. once the reaction gets going it provides its own starting materials. Such reactions are called "autocatalytic". Initially the oxidation takes place by a slightly different set of reactions, which dominate until sufficient HNO_2 has been formed for the above process to take off. An induction time would, therefore, be expected before the steady-state dissolution rate is achieved.

The silicon oxide is only sparingly soluble, so HF is used in the solution to form a water-soluble compound. A likely reaction is:

$$SiO_2 + 6HF = H_2SiF_6 + 2H_2O\,. \qquad (11)$$

Consider again the general equations for an oxidation-reduction process, Equations 1 and 2. If M is a semiconductor, the transfers of charge shown in the equations can take place by means either of electrons or of holes. If both processes use electrons, the overall reaction can be described as one in which an atom M leaves behind an electron which goes to another atom, X. If holes are involved, then the process is one in which M becomes a positive ion by removing a hole from the crystal, and X replaces it, i.e. Equations 1 and 2 might be more accurately represented by:

$$M + e^+ \rightarrow M^+ \qquad (1a)$$

$$X \rightarrow X^- + e^+\,. \qquad (2a)$$

Now suppose that the anode reaction takes place by Equation 1 and the cathode reaction uses Equation 2a. This is quite acceptable, since charge neutrality is maintained. The process now creates an electron-hole pair within the semiconductor for every atom that dissolves. This pair recombines within the recombination time for the semiconductor, but during etching the steady-state concentrations of carriers are increased. Similarly, the reaction might take place via Equations 1a and 2. In this case electron-hole pairs are destroyed during etching and the steady-state concentrations of carriers are depressed. Intermediate cases can occur between the two extremes, but the rule is that the same numbers of electrons and holes are either created or destroyed. This must be so in order to maintain charge neutrality. In the example given above for silicon, for instance, the oxidation reaction, Equation 5, is believed to occur by a silicon atom giving two conduction electrons to the lattice and taking two holes from it, thereby achieving the desired 4+ charge [2]. The reduction reaction, Equation 7, takes place using holes. Equation 7 must be doubled to make the chemical equations balance, so that four holes are given to the cathode for every silicon atom that leaves the anode. This means that each cycle donates two electrons and two holes to the semiconductor.

2.2. Effect of illumination

In those cases for which the concentrations of electrons and holes are depleted during etching, the supply of minority carriers to the semiconductor surface can become the factor that limits the rate of dissolution. The etching rate can then be increased by any mechanism that creates extra carriers at the surface, (e.g. illumination, which produces electron-hole pairs). A few etching processes are found to be sensitive to light in this way. Gatos and Lavine report, for example [3], that when germanium is etched in certain nitric acid solutions, the dissolution rates are doubled under strong illumination. It is important to realize, however, that any one of the processes involved in the dissolution might be the rate-limiting process. They will act in series, so the pace is that of the slowest. The limiting process might, therefore, be the supply of carriers to the surface, or any of the chemical reactions, or the processes to be described in the next section.

There are other ways in which illumination can affect the etching properties of the surface. Haisty [4] carried out some experiments etching n-type GaAs in KCl. He found that if a portion of the sample was illuminated, etching took place preferentially in that region. The following explanation was given. At the surface, the conduction and valence band edges of n–GaAs bend upwards so that the surface is, in fact, p-type. The effect of illuminating the surface is to bend the bands back a little. If part of the surface is illuminated and part dark, then the dark surface is more p-type than the rest. This gives rise to a photovoltage between the light and dark areas so that the illuminated GaAs becomes positive with respect to the rest. The anodic and cathodic reactions no longer take place randomly over the surface. The semiconductor behaves like an electrolytic cell, with the illuminated area as the anode and the dark area as cathode: virtually all of the dissolved material is, therefore, removed from the light area. Much the same effect has also been observed etching n-silicon in Dash etch [5], (see Appendix, Table AI).

The same mechanism can work for showing up a p–n junction, since a photovoltage develops between the p- and n-regions if a light is shone on the junction. p–n junctions are shown up in InP, for instance, if etched in potassium ferricyanide under illumination. Alternatively, a voltage can actually be applied to the junction.

2.3. Compound semiconductors

Chemical polishing of compound semiconductors also takes place by way of oxidation-reduction reactions, but much less information is available on the details of the reactions. Some work has been carried out determining the oxidation products of the III-V semiconductors. Poate *et al.* [6] oxidized GaP in H_2O_2 and analysed the resulting film using Rutherford scattering techniques. They decided the reaction product was probably a mixture of Ga_2O_3 and P_2O_5, although $GaPO_4$ may also have formed as well. Similar results were obtained by Schwartz [7] who oxidized GaAs and GaP in a variety of oxidizing agents.

The oxidation products can depend on the crystallographic orientation being polished. If a $\{1\,1\,1\}$ slice of GaAs is etched in nitric acid, for example, one side develops a dark stain and the other becomes quite shiny and shows etch pits. GaAs has the zinc blende structure, so one of the surfaces of a $\{1\,1\,1\}$ slice is composed of gallium atoms and the other surface is all arsenic (see Section 4.1). It has been shown [8] that the dark stain is due to crystals of As_2O_3 forming preferentially on the arsenic side of the slice. This, incidentally, provides a very useful way of identifying the two sides of a $\{1\,1\,1\}$ GaAs slice.

2.4. Addition of metal ions

Some etching solutions contain small additions of metal ions, the ones most commonly used being silver, chromium and iron in its ferric form. Some work has been carried out studying the chemical action of these ions [9, 88]. The ions do not usually change the overall etching rates of the solutions very much. However, solutions containing the ions do tend to show up more surface features than solutions without them. In particular, some solutions reveal certain dislocations only if metal ions are added. It seems likely that the explanation for this effect lies in the "dangling bands" that exist at dislocations (see Section 4.3). At the point of emergence of a dislocation there are more unsatisfied valence bonds than elsewhere on the surface, so a metal ion is more likely to be absorbed at such a point than elsewhere. It may then be able to take up one of the dangling electrons, thereby ionizing a surface atom. This should have the effect of increasing the dissolution rate at that point on the surface.

3. The dissolution process

3.1. Chemical and diffusion control

So far we have considered the chemical reactions that take place at the semiconductor surface. Since the reacting species are continually being used up in the reaction, it is necessary to consider the means whereby the species reach the surface, and also the means of removal of the reaction products. The transport mechanism can only be that of diffusion through the liquid and diffusion can, therefore, be the rate-limiting process for dissolution. As in Section 2, it must be noted that there is more than one process involved and the rate-limiting process will be the slowest of them. In practice it is convenient to describe a given dissolution process as being either reaction-rate limited (if one of the processes of Section 2 is the rate-limiting one) or diffusion limited.

Suppose a dissolution process is diffusion controlled, depending on the diffusion of some species to the surface. Assume that the species is used up as soon as it reaches the surface, so that the concentration there is zero. Let the concentration of the species in the bulk of the liquid be c. It is usual to assume that there is a layer, thickness δ, adjacent to the solid surface, in which the reactant is depleted. The rate at which the species reaches the surface, which is the same as the dissolution rate, can then be determined using Fick's law.

$$\frac{\mathrm{d}n}{\mathrm{d}t} = DA\frac{c}{\delta} \tag{12}$$

where A is the surface area of the sample, and D is the diffusion coefficient of the species in the liquid.

The value to give to A is not obvious. If the surface irregularities are small compared to δ, then A is the projected area of the surface. Since δ is likely to be of the order of tens of microns, this is usually the case. However, it is possible for δ to be less than this, either naturally, or artificially because of the liquid being stirred. In this case, δ might approach the size of the surface irregularities and A would approach the true surface area. Providing δ is fairly large so that A is the projected area, this argument implies that the rate of dissolution should be independent of the nature of the surface. This suggests a way of telling if a given dissolution process is diffusion or chemically controlled. If an etching solution etches different semiconductors at the same rate, then it is probable that the process is diffusion limited. Such etches do occur: a solution of Fe^{3+} ions in H_2SO_4 etches InSb, GaSb and InAs at approximately the same rate [3]. If an etch shows markedly different etching rates on different surfaces, on the other hand, it is almost certainly reaction-rate controlled. An etch consisting of 1 HCl:1 HNO_3, for instance, etches the $(\bar{1}\bar{1}\bar{1})$P surface of InP at a rate of 270 µg cm^{-2} sec^{-1} and the (1 1 1)In surface of the same semiconductor at 4 µg cm^{-2} sec^{-1} [10].

Probably a more reliable way of deciding whether a process is chemically or diffusion controlled is to determine the activation energy for the process by measuring the dissolution rate as a function of temperature, T. If a graph of rate versus T^{-1} gives a straight line, then an activation energy can be calculated. In general, the activation energy for a diffusion process is less than that for a chemical reaction in the type of system under discussion [11]. For semiconductor dissolution, activation energies for diffusion are less than about 7 kcal mol^{-1}. The etch consisting of Fe^{3+} ions in H_2SO_4 mentioned above, for instance, was found to operate with an activation energy of about 5 kcal mol^{-1}, confirming that the process was diffusion limited. Experimentally, the determination of activation energies requires care. If the chemical reaction generates heat, the local temperature at the semiconductor surface is likely to be quite different from the measured temperature in the bulk of the etch.

The limiting process can change with a change in etching conditions. Fig. 1 shows the etch rate versus temperature data for silicon in an etch consisting of $3HNO_3$;1HF:$1H_2O$ plus a small addition of $NaNO_3$ [12]. The graph shows two straight-line branches, indicating a high activation energy below about 20°C and a lower one above this temperature. It is reasonable to assume that different rate-limiting processes operate above and below 20°C.

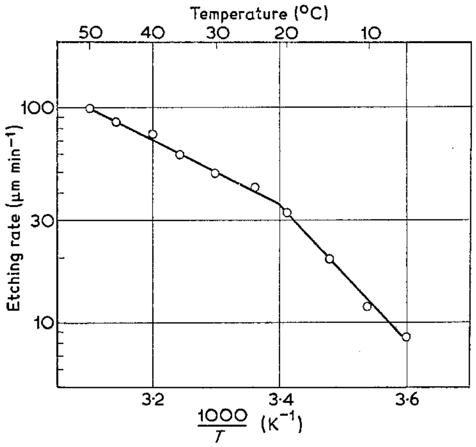

Figure 1 Etching rate of silicon as a function of temperature in an etch consisting of $3HNO_3$:1HF:$1H_2O$ plus a small addition of $NaNO_3$ (see [12]).

The rate-limiting process can also be altered by changing the relative proportions of the constituents in a given etching system. Robbins and Schwartz carried out a comprehensive series of experiments in which they etched silicon in mixtures of HNO_3:HF:CH_3COOH of various compositions [12, 13]. Fig. 2 shows curves of constant etch rate at 25°C, plotted on a composition diagram. The shapes of these curves are very revealing. In the region of high HNO_3 concentration, for instance, the constant-etching lines are parallel to the nitric-acetic acid base line, i.e. they are lines of constant HF composition. It follows that the determining factor in the dissolution rate is the amount of HF in the etch. At 25°C, the activation energy in this composition region was found to be about 4 kcal mol^{-1}, i.e. an energy indicative of a diffusion process. Therefore, in the high HNO_3 region of

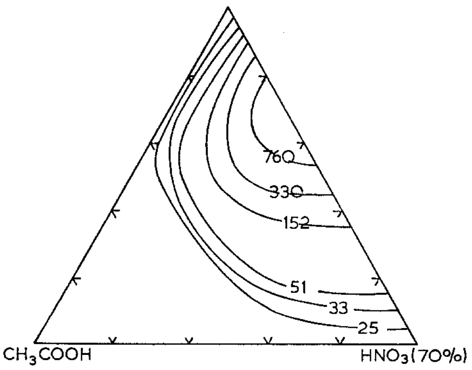

Figure 2 Constant etch-rate curves for silicon in the system HNO_3:HF:CH_3COOH, at 25°C. The numbers on the curves indicate etch-rate in µm min^{-1} (see [13]).

the diagram, the limiting process is the diffusion of HF to the semiconductor surface. For those etches with very low HF concentrations, the etching rates are very small, because of the low rate of removal of the SiO_2 that is formed. In the extreme, a layer of oxide builds upon the surface and complete passivation of the etching process can occur.

In the region of high HF concentration on the composition diagram, the curves are lines of constant HNO_3 content, so the etching rate is determined by the amount of nitric acid in the etch. The activation energy is higher than in the previous case, indicating chemical control. The rate-limiting process is, therefore, one of the chemical reactions involved in the oxidation of silicon by nitric acid (i.e. Equations 4 to 8).

If a given etching solution is diffusion controlled, it has a low activation energy and the etching rate is, therefore, relatively insensitive to variations in temperature. This can be an advantage if a highly reproducible etching process is required. A chemically-controlled process, on the other hand, requires much closer temperature control. Variations in the etching rate of a diffusion controlled system can be achieved by adding some liquid to the etch, which has the effect of making the solution more viscous. The diffusion coefficient of the reactants and, therefore, the rate of dissolution, is then reduced. This was demonstrated in a elegant way by Bogenschutz *et al.* [14], who studied the etching of germanium and silicon in a HNO_3–HF–CH_3COOH mixture. They plotted activation energies in a manner similar to that of Robbins and Schwartz, and found activation energies of 4.72 kcal mol^{-1} for silicon and 4.96 kcal mol^{-1} for germanium. Note that these values imply a diffusion-limited process both because of the low values of the energies and because of the fact that two different semiconductors gave essentially the same value. They also measured the viscosity of the polishing solution as a function of temperature and found the activation energy to have approximately the same value at $-$ 4.60 kcal mol^{-1}. (The negative sign indicates that viscosity decreases as temperature increases.) The result shows quite clearly that the etching rate was determined by the viscosity of the solution.

3.2. Effect of stirring solutions

Agitating a chemical polishing solution often changes the dissolution rate of the semiconductor. The effect on a diffusion-activated process is, in general, different to that on a chemically-activated one. Stirring can, therefore be used to help decide what type of process is rate-limiting. Many ways of stirring are used in practice: one of the most convenient is to have the semiconductor slice in the bottom of a beaker of etch, which is rotating on its axis. The beaker is also tilted at some angle to the vertical so that the semiconductor slice turns like a wheel in the bottom of the beaker. This arrangement gives a steady flow of liquid over the slice. Alternatively, a mechanical stirrer can be used in the liquid.

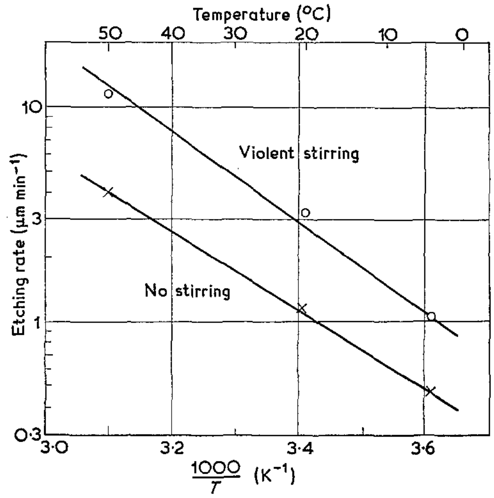

Figure 3 Etch rate as a function of temperature for GaAs, with and without stirring. The etching solution consisted of $1H_2O_2{:}8H_2SO_4{:}1H_2O$ (see [15]).

If the dissolution is diffusion-limited, the effect of stirring is to reduce the thickness of the depleted layer, δ, in Equation 12. The etching rate is therefore increased. An example of a diffusion-controlled system that has an increased dissolution rate when stirring is applied is given by Iida and Ito [15]. They studied the dissolution of GaAs in the system H_2O_2–H_2SO_4–H_2O. Fig. 3 shows the effect of stirring on a mixture of $1H_2O_2{:}8H_2SO_4{:}1H_2O$. A factor of about three is gained when the liquid is stirred violently. Note, however, that the slope of the graph is not changed by the stirring. The activation energy is therefore the same, and the rate-limiting mechanism is still diffusion. Compositions of this mixture containing smaller amounts of sulphuric acid gave larger activation energies. This suggests that such compositions have a chemical rate-limiting process. According to the argument given above, it would be expected that stirring would have little effect for these compositions. This was found to be so by Iida and Ito.

Some dissolution reactions produce bubbling at the semiconductor surface and this provides a very effective "natural" means of stirring the liquid. If the bubbling is at all vigorous, it is unlikely that any externally applied form of stirring will produce an effect comparable to the naturally-occurring one. Under these circumstances it is not possible to increase the rate of dissolution of a diffusion-limited process by stirring the liquid.

In general, stirring will not change the dissolution rate of a chemically limited process, since there is no problem here about supplying material to the semiconductor surface: the constriction in the pipeline is chemical reaction at the surface. (On the other hand, stirring could conceivably turn a diffusion-limited process into a chemically-limited one). If the limiting process is an autocatalytic reaction, such as that described in Section 2.1, however, then stirring does have an effect. In this case the reaction products at the surface are required to catalyse the reaction. Stirring tends to remove these products from the reaction area and therefore decreases the etching rate.

3.3. Combination of mechanical and chemical polishing

Mechanical polishing of semiconductors is usually carried out using very fine abrasive particles of diamond or alumina, suspended in a lubricant. Very high quality surface finishes can be produced in this way. The disadvantage with the method is that the surface which is produced is damaged (see Section 4.5). Chemical polishing, on the other hand, produces a surface which is damage-free but is often not very flat. A combination of the two methods can be used which gives a damage-free surface of very high quality. The technique [16-18] is simply to polish the semiconductor slice on a polishing cloth soaked in the etchant (no abrasive particles are used). This can be done either manually or using a polishing machine. Reisman and Rohr [18] obtained high quality surfaces on germanium and GaAs. They explained their results by a consideration of the effect of the pile of the polishing cloth on the flow of etchant over the surface. Providing the pile is not too long, turbulence occurs at any protrusions, which then etch faster.

Hartnagel and Weiss [16], polishing GaAs in a $NaOCl:H_2O$ solution, studied the effect of varying the pressure on the semiconductor and found an increase in polishing rate for greater pressure. They also found an interesting additional effect due to the mechanical polishing action. If the GaAs was simply suspended in a solution of the etchant, with no polishing pad present, polishing proceeded only for about 1 min. An insoluble film then formed on the semiconductor, which stopped the process. When mechanical polishing was used as well, however, this layer was continually removed, allowing polishing to proceed.

Another technique which looks similar but is, strictly speaking, not mechanical polishing at all, is used in the polishing machine of Sullivan *et al.* In this apparatus the semiconductor slice is held parallel and close to a large rotating disc. Etchant is dropped between disc and semiconductor. The effect is to produce a very vigorous stirring action of the etchant. The slice must be held far enough from the disc to make sure it never touches and yet is close enough to maintain a film of etchant in the gap. Very high quality surfaces have been produced in this way on silicon and germanium [19], GaAs [20] and CdS [21].

4. Crystallographic effects

4.1. Surface orientation

When semiconductors are etched in certain solutions, it is found that some crystallographic planes etch faster than others. An elegant way of demonstrating this phenomenon is to immerse a single crystal sphere in the solution. If the etching is non-preferential, the sphere gets smaller but does not change shape. If the system etches different planes at different rates, however, a polyhedron is obtained on which the fast-etching planes form the sides and the corners correspond to orientations giving etching rate maxima. If, for instance, a sphere of GaAs is etched in a solution of $3HNO_3:1HF:0\text{–}4H_2O:1\%\ AgNO_3$, a rhombic dodecahedron is formed, bounded by $\{110\}$ faces [22]. Similar results have been reported for silicon [23], [83] germanium [24] and InSb [25].

For different rates to be obtained in this way, the etching must be determined by the nature of the surface, i.e. the rate limiting process is a chemical reaction involving surface atoms. (It has been pointed out in Section 3 that a diffusion-limited process would etch all faces at the same rate.) Surface atoms are not as completely bonded to the crystal as are interior atoms: there are, therefore, a number of "free" bonds, available at the surface to take part in a reaction. The number of these bonds per unit area is slightly different for faces of different orientations, and it has been proposed that it is this effect that causes the differences in etching rates [3]. Harvey and Gatos [26] have tested this idea, etching germanium in oxygen-saturated water. They carried out their experiments on {100}, {110} and {111} material and also calculated the concentrations of free bonds on the surface for those orientations. Their results are shown in Table I. It can be seen that the relative etching rates agree quite well with the relative densities of free surface bonds.

TABLE I Densities of free bonds on germanium surfaces, and dissolution rates in oxygen-saturated water [26]

Orientation	Free bonds (cm^{-2})	Relative free bond density	Relative etch rate
{100}	1.25×10^{15}	1.00	1.00
{110}	8.83×10^{14}	0.71	0.89
{111}	7.22×10^{14}	0.58	0.62

Very much larger surface orientation effects can be obtained with compound semiconductors, essentially because more variation is possible in the different surfaces. Consider, for example, the zinc blende crystal structure, which is the one possessed by most of the III-V semiconductors and also by some I-VII and II-VI compounds. Call the compound AB and, to fix ideas, let A be a group III element and B a group V. The zinc blende structure can be thought of as a series of parallel {111} planes made up alternately of A and B atoms. The planes are bonded alternately by sets of three bonds and sets of a single bond. The arrangement is shown diagrammatically in Fig. 4. Now suppose that a slice is prepared with {111}-type faces. When the material is sliced, it is the layers joined by the single bonding that are separated rather than layers joined by triple bonding. This gives rise to one of the two surfaces being composed completely of A atoms. Call this surface (111). The other surface is made up entirely of B atoms. Call it $(\bar{1}\bar{1}\bar{1})$. X-ray techniques have been developed to differentiate these two types of surface [27, 28].

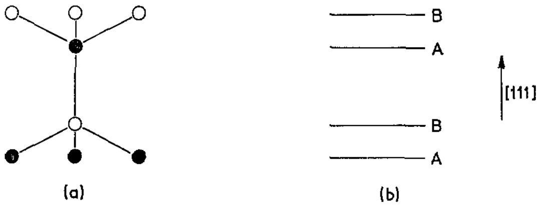

Figure 4 (a) Bonding in the zinc blende structure. In three dimensions, all bonds are of equal length and are at equal angles to each other. (b) Arrangement of (111) planes in a [111] direction in zinc blende.

There is an important difference between the two sorts of {111} surface. Assuming the surface atoms are electrically neutral, each A surface atom has three bonding electrons and each B atom has five. Three bonds are used up in holding on to the crystal (see Fig. 4a). The A atoms, therefore, have no "free" electrons at the surface. The B atoms, however, have two electrons that can easily take part in any reaction. Accordingly, a $(\bar{1}\bar{1}\bar{1})$ surface should be more chemically active than a (111) surface. Other surface orientations have different surface structures. The {100} surfaces in zinc blende, for instance, can, in principle, consist either of A or B atoms, both types being doubly bonded to the lattice. Since neither is preferred, a real {100} surface consists of a mixture of A and B atoms. From the argument given above, one can predict that a (100) surface etches faster than (111) but slower than $(\bar{1}\bar{1}\bar{1})$, in an etching solution that is limited by chemical reaction. This prediction has been tested and confirmed for InP [10] and InSb [29]. An example, for InP, is shown in Fig. 5, which gives etching rates for three orientations of the semiconductor when etched in concentrated HCl. The steady etching rates are in the expected order: the enhanced rates close to the surface are discussed in Section 4.5.

A similar story can be told about the wurtzite structure which is the crystal form of the II-VI semiconductors CdS and CdSe. As in the zinc blende structure the crystal consists of layers of A and B atoms held together by sets of single bonds alternating with sets of three bonds (see Fig. 4a). The only difference between wurtzite and zinc blende is in the stacking sequence of the layers. In the former, the layers are stacked in such a way as to create a hexagonal-type structure, with the parallel layers of Fig. 4 now becoming basal {0001} planes. Thus a {0001} slice of CdS has an (0001) face consisting of

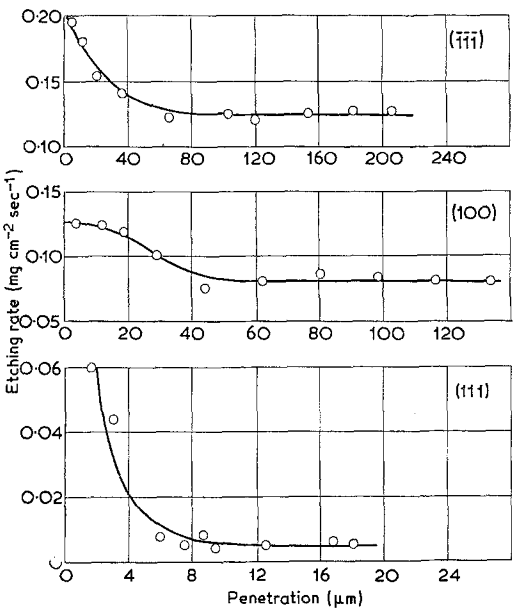

Figure 5 Etch rates versus penetration for various orientations of InP. The etch used was conc. HCl at 26°C (see [10]).

cadmium atoms and a $(000\bar{1})$ face of sulphur atoms. As might be expected, it is found that the two types of face exhibit different etching properties, although the difference is usually not as marked as that shown by zinc blende semiconductors. The different faces can be identified absolutely using X-ray techniques [30].

The difference in chemical behaviour of A and B surfaces has been discussed so far in terms of the concentrations of available bonds at the respective surfaces. There is one other difference that may well be important, however. It has been pointed out that large differences in electronegativity exist between the components of some of the II-VI compounds [30]. This is especially true of ZnS (zinc blende), ZnSe (usually zinc blende, but can take the hexagonal form), CdS and CdSe (both wurtzite). The A components (Zn, Cd) have larger electronegativities than the B components (Se, S) [31], and it seems reasonable to assume that at least some of the difference in behaviour between A and B surfaces in these compounds is due to this fact.

4.2. Surface background structures

Some etches produce a semiconductor surface that is optically flat. Most surfaces produced by chemical polishes, however, show features that are visible under the microscope and it is interesting to consider what causes them. Background structures can arise if there are large differences in etching rates between the various crystallographic planes of the crystal. Suppose, for the sake of argument, that we etch a (1 1 1) plane. Real crystal surfaces are not, in general, perfectly flat, and at the microscopic level the crystal will actually consist of a rough surface displaying a wide variety of crystal planes. The average of all these planes will, of course, be (1 1 1). If the etching rates of these facets vary by very much, then complex crystallographic features can appear on the surface. The conditions for the stability of both convex and concave structures on the surface have been discussed at some length by Irving [32] and by Batterman [33]. Some of these structures, many of which can be quite beautiful, are only metastable, however, and are removed by prolonged etching. An example of a background structure which is probably due to differences in etching rate is shown in Fig. 6. The figure shows a scanning electron microscope picture of a (1 1 1)In surface of InP etched in concentrated HCl. This does appear to be a stable structure: the appearance does not change for etching times between 2 and 20 min [10]. The data of Fig. 5 confirm that this etching system is indeed one which demonstrates a large variation in etching rates for different orientations.

Background structures such as that of Fig. 6 should only appear in systems which operate under chemical activation, since diffusion-limited

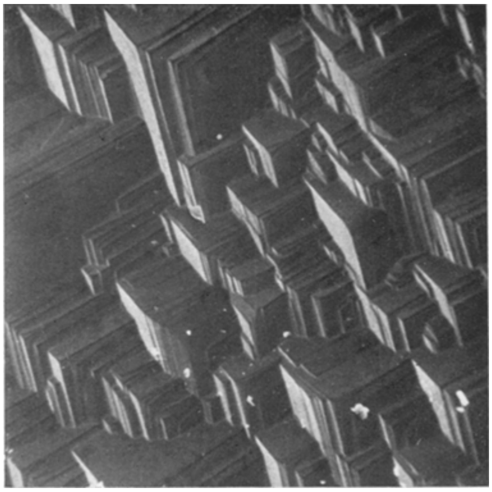

Figure 6 (1 1 1) surface of InP etched in conc. HCl for 20 min × 300 (see [10]).

systems etch all surfaces at the same rate. Structures are sometimes observed in diffusion-limited systems, but they do not usually exhibit the sharply crystallographic features of Fig. 6. They are probably due to local variations in diffusion, caused by currents in the etching liquid, i.e. they depend on the local flow of etchant over the surface.

4.3. Etch pits

As well as the general background structures observed on etched semiconductors, individual features are commonly observed, notably pits and hillocks. A pit will form at a point on the surface if the dissolution rate is enhanced at that point relative to elsewhere on the surface. This enhancement can take place either because of a random process or because of some special property of the crystal at that point. An example of the first type of enhancement is seen in systems in which the chemical reaction is a violent one forming bubbles of gas on the surface. In this type of reaction, large amounts of semiconductor are removed and the surface becomes covered with pits (perhaps better described as "holes").

The most important etch pit of the second type is the one associated with the point of emergence of a dislocation on the surface. There are a number of reasons why these points might have an enhanced dissolution rate:

(i) There is an elastic strain field around a dislocation and this might lead to a higher chemical activity. This mechanism may well operate in certain cases. However, it is difficult to see how it can operate in those cases for which a given dislocation causes an etch pit if it intersects one crystal plane, but not if it intersects another (see below).

(ii) The higher rate might be associated with a higher impurity concentration at the dislocation. During crystal growth, impurity atoms tend to migrate to dislocations because they fit more easily into the lattice there, i.e. it is a low-energy configuration.

While it seems likely that this mechanism operates for some etching systems, there is evidence to suggest that dislocation etch pits can occur associated with dislocations which probably do not have a high concentration of impurity atoms. It is a fairly simple matter to introduce dislocations into a semiconductor crystal by mechanical means. If, for instance, a crystal is bent, the bending is accommodated by the crystal creating a large number of edge dislocations of the same sign. It is possible in this way to create a large number of dislocations in a rather short time. The crystal slice is put under an appropriate stress and a current of several amps is passed through. The crystal is raised to about 800° C and bends under the action of the applied stress. The whole procedure takes 10 to 100 sec (see for instance [90] using silicon and [91] using GaAs). The dislocations formed in this way can give rise to dislocation etch pits without any further annealing of the specimen. If these pits are due to an enhanced impurity atmosphere at a dislocation, impurities already present in the semiconductor must have diffused to the dislocation. The diffusion would have had to occur after the formation of the dislocations, but before the specimen temperature became too low for significant diffusion to occur. Bearing in mind that most of the 10 to 100 sec would be taken up in heating the specimen before it bends, the time available for the atoms to migrate to the dislocations would be no more than a few seconds. It seems unlikely that this would be long enough, given the likely diffusion coefficients at the bending temperatures employed. This cannot be stated with certainty, however, because too little information is available on the forces of attraction between dislocations and impurities.

Experiments on dislocation decoration are relevant here. Decoration is a term used to describe the precipitation of impurities on dislocations (see below). If decoration is not observed experimentally, it does not mean that no migration of impurities to dislocations has taken place, merely that it has not occurred on a large enough scale to give visible precipitates. It is worth noting, however, that Abrahams and Buiocchi [36] had to anneal GaAs for 120 h to decorate dislocations introduced by bending. similarly, Bullough *et al.* [102] annealed silicon doped with boron and phosphorus for many hours without observing decoration of dislocations.

There is also evidence to suggest that dislocation loops can be formed during mechanical abrasion of a semiconductor surface [92-94]. Such surfaces can give rise to etch pits [e.g. 95]. It seems unlikely that diffusion temperatures are achieved at the surface of a semiconductor during the mechanical polishing process although, once again, there is too little evidence to be dogmatic about it.

(iii) A simple hypothesis to account for etching of edge dislocations has been put forward by Gatos and Lavine [34]. It is based on the "dangling bond" model of an edge dislocation due to Read [96]. According to this model each atom on an edge dislocation has a dangling bond because it is not as completely bonded to the lattice as a normal atom. There is thus a line of unsatisfied bonds along a dislocation. At the point where the dislocation intersects a surface, this can lead to an extra free bond at the surface, and hence greater chemical activity.

It is of interest to apply this explanation to the specific case of the zinc blende lattice. The "extra half-plane" of a dislocation in this structure terminates either on a row of A atoms or on a row of B atoms. Call these dislocations α- and β-types respectively. Consider the points of intersection of these dislocations with the $\{111\}$ surfaces. The dislocations can intersect both the A(1 1 1) face and the B($\bar{1}\,\bar{1}\,\bar{1}$) face. There are, therefore, four types of intersection which could possibly lead to etch pits – call these Aα, Aβ, Bα, Bβ. Gatos and Lavine considered the bonding at these four intersections and concluded that at only one of them, Aα, is the bonding configuration likely to lead to an enhanced etching rate. This conclusion was confirmed for a number of etches on several III-V compounds [34, 35]. Subsequent work on InSb by Lavine *et al.* [9] and by Bell and Willoughby [97], has shown, however, that all four types of dislocation can be revealed in this material using suitable etches. Most of this latter group of etches involved the addition of surface active agents such as metal ions or organic sulphides. Similar results were obtained for GaAs, using solutions containing metal ions [36].

Probably all three of these mechanisms operate on different etching systems. Abrahams and Buiocchi [36], for example, bent GaAs samples and etched them in a solution composed of CrO_3, HF, $AgNO_3$ and H_2O (see Table A2). They found that β dislocations produced etch pits, and α dislocations did not. After annealing for 120 h at 1100°C, however, both types gave etch pits. They accounted for this by suggesting that in their etching system, α dislocation etch pits formed only if the dislocations were decorated with impurities: β pits formed without being decorated. During the long anneal, impurities migrated to the dislocations. Pits could then be formed by the α dislocations.

Perhaps the most important point to note from this is that although an etch may show up dislocations, it does not necessarily show up all of those intersecting the surface. In particular, it seems to be much easier to reveal edge dislocations than screw, although there is clear evidence that screw dislocations can give rise to etch pits in germanium [98]. Similarly, dislocations of a given type may produce etch pits on one crystal plane but not on another.

The other side of the coin is that etch pits can occur which are not associated with dislocations. Precipitates in the surface, for instance, might cause an increase in dissolution rate. The point is of some importance. If in a given etching system we can unambiguously identify etch pits with dislocations, we have a simple and powerful technique for studying dislocation densities and other properties such as the velocity of a dislocation when it moves under the action of a force [99]. Several techniques can be used to confirm that a pit indicates the point of mergence of a dislocation. Perhaps the simplest is to etch a surface, grind some of it away and then re-etch. The process is then repeated. If the same pattern of pits is revealed at each re-etching step, the defects must be lines leading from the surface. Is is reasonable to assume in this case that they are dislocations.

Other techniques used to identify pits with dislocations involve making the dislocations visible. If this can be done, it is a simple matter to see if the points of intersection with the surface correspond to the etch pits. Dislocations can be made visible using X-ray topography (see for instance, the review articles by Alexander and Haasen [99] and Amelinckx [100]). Another technique, decoration, was first used by Dash [101] to reveal dislocations in silicon. The technique relies on the fact that silicon is transparent to infra-red light. Copper is diffused into the silicon for long enough for it to become distributed throughout the specimen. The crystal is then cooled from the diffusion temperature over a time of several minutes. During the cooling process, the copper precipitates out on the dislocations. When viewed under infra-red light, the lines of precipitate are opaque, and the dislocation lines are revealed. The decoration technique requires an impurity which can diffuse very rapidly to the dislocations. Copper is usually used: it diffuses interstitially in many semiconductors, with a high diffusion coefficient. As mentioned above, Bullough *et al.* [102] attempted the same experiment using phosphorus

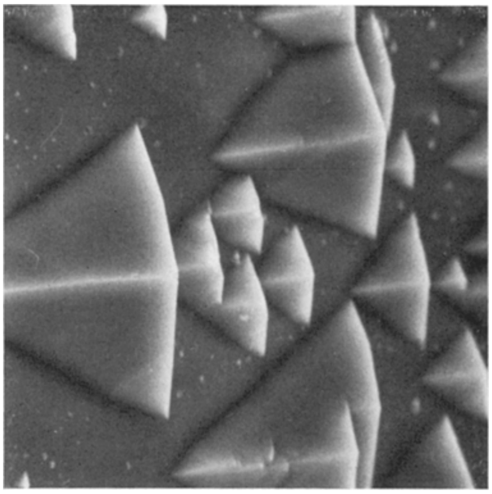

Figure 7 Etch hillocks on a $(\bar{1}\bar{1}\bar{1})$P surface of InP. The etch was 1HCl:1HNO_3, used for 2 min, × 3200 (see [10]).

and boron in silicon. They observed no precipitates on the dislocations, presumably due to the relatively low diffusion coefficients of phosphorus and boron in that semiconductor.

4.4. Etch hillocks

Hillocks appear less often than etch pits, but are by no means uncommon. They have been reported as occurring on germanium [33], InP [10], SiC [37] and GaAs [38]. A fairly typical example is shown in Fig. 7, which is a scanning electron microscope picture of a $(\bar{1}\bar{1}\bar{1})$ surface of InP etched for 2 min in 1HCl:1HNO_3 solution. It is worth noting the complete lack of surface structure between the hillocks.

Hillocks must correspond to points on the surface where dissolution is inhibited. Patel and Mathai have presented evidence to suggest that the features they observed on SiC corresponded to dislocations [37]. Batterman's studies, on the other hand, led him to believe that hillock formation in germanium is not related to internal structure but is a surface-nucleated phenomenon. He noted that a surface kept free of contamination produced very few hillocks [33]. A more recent study on GaAs tends to confirm this view [38]. A scanning electron microscope study of etch hillocks in this material showed that the tops of the hillocks were invariably coated with a flaking layer of material, presumably a reaction product. There seems to be a good deal of scope for further work investigating these features.

4.5. Work damage

Prior to etching, a semiconductor is usually in the form of a thin slice that has been cut from a larger single crystal. Quite often the surfaces have been abraded to produce a shiny finish. It is commonly found that when a sample of this sort is etched, the initial rate of etching is greater than the final steady rate. The effect is shown quite well in Fig. 5. It is generally agreed that the high etching rate is due to the damaged nature of the material just below the surface. The process of abrasion can produce a variety of defects in this layer, which increase the chemical activity of the material. Etching data such as that shown in Fig. 5 represent a simple means of estimating the depth of damage, by noting the depth below the surface at which the steady-state etching rate is achieved. Estimates of abrasion-depth found using this method have been compared with measurements taken by other methods, such as X-ray rocking curve half-width [39]. They are in good agreement.

Another interesting feature of the results of Fig. 5 is that the depths of damage are different for the different orientations. The order is $(\bar{1}\bar{1}\bar{1})$P > (100) > (111)In. The same result was found for two other InP etches [10]. Similar results have been reported by Gatos *et al.* for InSb. They came to the conclusion that for this material the same abrasive treatment produced depths of polishing damage in the order (100) > $(\bar{1}\bar{1}\bar{1})$Sb > (110) ⩾ (111)In [40].

5. Polishing solutions

In this section a few general remarks are made about the etching solutions that have been used for semiconductors of groups IV, III-V and II-VI. In addition, a brief account is given of some of the more comprehensive investigations that have been carried out. Specific etching solutions are listed in the Appendix.

5.1. Group IV semiconductors

By far the largest body of work in this subject is that concerned with the polishing action of nitric acid solutions on silicon and germanium. The chemical aspects of the oxidation-reduction reaction, outlined in Section 2.1, have been discussed in detail by several workers, both for silicon [12, 13, 41-43] and germanium [44-46]. Most of these investigations used HF as a complexing agent. A good deal of experimental data are now available for these systems. Schwartz and Robbins carried out an extensive series of experiments etching silicon in HNO_3–HF–H_2O and HNO_3–HF–CH_3COOH [12, 13, 41]. They measured the etch rates over a wide range of composition for the two types of solution; graphs of etch rate versus temperature were produced for a number of compositions and activation energies were calculated. They also carried out similar work polishing germanium in HNO_3–HF–CH_3COOH. The effect of rotation on the water-diluted system was investigated by Klein and D'Stefan [43] for silicon. Etching of both silicon and germanium in the HNO_3–HF–CH_3COOH system has been investigated by Borgenschutz *et al.* [14], who compared activation energies for etching with those for diffusion. Data on activation energies for the dissolution of germanium in a variety of compositions of HNO_3–HF–H_2O have also been presented by Burgess [47].

It is worth noting that included in the general class of nitric acid solutions is CP4, one of the most commonly-used semiconductor etching solutions (see Appendix, Table A1).

Hu and Kerr [84] have shown that silicon can be etched in solutions made up simply of HF and water. The etch rates are very low, however, of the order of 1 Å min^{-1}. They carried out a series of experiments in which the concentration of $(OH)^-$ ions was varied and the etching rate measured. As a result of their work, they came to the conclusion that the etching action was probably caused by the oxidation of silicon by the hydroxyl ions in the aqueous solution.

A number of rather more exotic etching solutions for silicon was investigated by Finne and Klein [85]. They used ternary solutions made up of water, amine and a complexing agent. Most of their work used ethylenediamine ($NH_2(CH_2)_2NH_2$) and a complexing agent of pyrocatechol ($C_6H_4(OH)_2$). They suggest the following reaction mechanism. The amine reacts with water to form $(OH)^-$ ions, which oxidize the silicon. The pyrocatechol then reacts with the oxidized semiconductor to form a product which is soluble in the amine solution. Finne and Klein claim great flexibility for this etching system. A large variation in etching rate can be achieved by varying the proportions of the constituents. In addition, the etch has a very low rate of attack on silica and on various metals such as silver, gold, copper and tantalum, all of which can, therefore, be used as masks.

An important group of etchants for germanium is that based on the use of H_2O_2 as the oxidizing agent. It was shown by Primak *et al.* [48] that dilute H_2O_2 etches germanium very slowly. Higher rates were obtained by Bloem and van Vessem [49], who presented etch rate versus composition diagrams for the H_2O_2–HF–H_2O system. Similar experiments were carried out by Schwartz [50], who also measured the etch rates of a number of compositions as a function of temperature. It has been shown that certain compositions of this system can produce hillocks on germanium (e.g. "Superoxol": see Appendix, Table A1).

More recently the peroxide system has been investigated using complexing agents other than HF. A number of liquids were found suitable, including tartaric, acetic, citric, oxalic and hydrochloric acids [45].

The other important group IV semiconductor is SiC. This is a difficult material to work with and very little data on its etching properties are available. It can assume either a cubic or hexagonal type of crystal structure and is often a mixture of the two. It is a high-melting-point material and it is found that most etches have to be used at high temperatures in order to be useful. A review of the etching properties of SiC has been given by Brander and Boughey [51]. Patel and Mathai [37] have shown that etch hillocks are formed by a solution of NaOH and KNO_3 at 630°C. See Appendix, Table A1 for further details.

5.2. III-V semiconductors

Some of the chemical etches used for the III-V materials are similar to those described for silicon and germanium. There is a group of solutions based on the use of nitric acid as an oxidizing agent, and another which uses H_2O_2. Hydrofluoric acid is also much in evidence as a complexing agent. One of the most useful etches consists of a few per cent of bromine in methanol. This solution was first used by Fuller and Allison [52] for GaAs, but can be used for most III-V semiconductors. A very high quality polish can often be obtained using this etch.

Although a good deal of work has been carried out observing the effects of various polishing solutions on III-V semiconductors, there are not many large-scale studies of a single system, as there are for silicon for instance. Probably the largest body of work is that on InSb, put together by Gatos and his co-workers [9, 29, 34, 40]. They investigated the etching properties of $\{100\}$, $\{110\}$ and $\{111\}$ surfaces using a variety of etching solutions based on nitric acid, H_2O_2 and Fe^{3+} ions as oxidizing agents. They also added various surface active agents to their basic etching solutions and observed the change in etching behaviour produced. The effect of surface damage on etching rates was observed.

A comprehensive series of experiments etching {100} GaAs in H_2O–H_2SO_4–H_2O has been reported by Iida and Ito [15]. They measured the etching rate over the complete range of compositions for the three constituents. They also presented curves showing how the etching rates vary with temperature and investigated the effect of vigorously stirring the etchant.

The bromine-methanol system has been investigated for GaAs by Tarui *et al.* [53]. They showed that the etching rate increases with increasing bromine concentration up to about 5% by weight of bromine. The rate then starts to level off. They also showed that different crystal faces etch at different rates, with the rates for a 1% bromine solution in the order $(110) > (\bar{1}\bar{1}\bar{1})\mathrm{As} > (100) > (111)\mathrm{Ga}$.

The chemistry of the dissolution processes involved in etching of III-Vs is more complicated than that for silicon and germanium. A good deal more work needs to be done in this area before it is understood. Interesting work has been carried out investigating the nature of the oxide product of the reactions, mostly using GaAs and GaP. Schwartz has oxidized both of these semiconductors, using a number of agents [7]. The resulting surface films were observed using X-ray and electron diffraction techniques, and were identified in some cases. Oxide films in these materials have also been analysed using chemical analysis [54] and Rutherford back-scattering [6] (see also Section 2.3).

Further details of etching solutions used for III-V semiconductors are given in Table A2 of the Appendix.

5.3. II-VI semiconductors

Once again both HNO_3 and H_2O_2 are used as oxidizing agents in a number of etches. The bromine-methanol etch can be used for several of the II-VI compounds [55]. Warekois *et al.* etched a number of these semiconductors in several different etches and established that the A-type basal planes have different etching properties to the B-type. Details of a number of etching solutions are given in Table A3 of the Appendix.

6. Conclusions

While it is true that there is a great deal of data in the literature giving the effects of specific chemical mixtures on semiconductors, it is also true that relatively few systematic investigations have been carried out studying etching systems in detail. Work is required in which a whole range of data is collected for a given system. This involves varying the composition of the etch, measuring activation energies, observing the effect of stirring, noting the action of the etch on different faces of the same semiconductor, etc. There are many etching systems that are very important (in the sense that they are widely used), for which work of this type has not been carried out. This is especially true for the compound semiconductors. There seems, also, to be a special need for the chemical reactions involved to be studied more thoroughly. Until more work of this sort is carried out, chemical polishing will remain something of an art.

Finally it must be noted that many of us who deal in the polishing of semiconductors do so with a somewhat limited knowledge of chemistry. Many liquid mixtures are capable of producing highly explosive solutions (nitroglycerine comes to mind). Many more are harmful if allowed to come into contact with the skin. An article in *J. Electrochem. Soc.* [56] mentions a number of chemicals that should be treated with respect: it also advises all workers in this field to take the greatest care when trying out a new etch. This is obviously good advice.

7. Appendix

A number of etches that have been used for semiconductors of groups IV, III-V and II-VI are given in the following tables. So many variations have been mentioned in the literature that the list is, of necessity, selective. Lists of semiconductor etches have also been produced by Gatos and Lavine [3] and by Holmes [57].

TABLE A1 Etches for group IV semiconductors

	Semiconductor	Etchant	Remarks	Reference
1	Si	$5HNO_3$ $3HF$ $3CH_3COOH$	Usually called CP4A. Produces polished surface in 2-3 min	58
2		$3HNO_3$ $1HF$ 8-12 CH_3COOH	Called Dash etch. Gives rise to deep dislocation etch pits. Takes several hours	59 60
3		0.5-0.1% HNO_3 in HF	Applied under a strong light. Shows up p–n junctions by turning p-type darker than p-type	61
4		NaOH or KOH 1-30% solution	Applied for 1-5 min at 50-100°C it develops etch figures	62 63
5		H_2O 8 ml $NH_2(CH_2)_2NH_2$ 17 ml $C_6H_4(OH)_2$ 3 g	Does not attack silicon oxide. Etches {100}, {110}, {111} planes at 50, 30, 3 µm h^{-1} respectively. See Section 5.1	85
6	Ge	$25HNO_3$ $15HF$ $15CH_3COOH$ with 0.3 Br_2 dissolved	Called CP4. Gives a polished surface in about 2 min	64
7		As etch 1	Slower etch than 6	
8		10 HNO_3 5 HF 11 acetic acid with 30 mg I_2 dissolved	More satisfactory for (100) surfaces than CP4	65
9		1 H_2O_2 1 HF 4 H_2O	Called Superoxol. Develops etch figures	33 66
10	SiC	Fused KOH or NaOH	Temperatures in excess of 600°C	67
11		Fused Na_2O_2	Used between 350 and 900°C. Rapid removal of material at the higher temperature	67
12		Equal volumes of aqueous NaOH and $K_3Fe(CN)_6$	Etching at the boiling point (110°C). Differentiates between (0001) and $(000\bar{1})$ in SiC	68

TABLE A2 Etches for III-V semiconductors

	Semiconductor	Etchant	Remarks	Reference
1	GaAs	1-20% Br_2 in CH_3OH	Polished surface	52
2		3 HNO_3 2 H_2O 1 HF	Polishing with rapid removal of material. Can be slowed down by doubling amount of water. When used in this diluted form under illumination, it shows up growth striations	22 87
3		1 H_2O_2 1 HF 1 H_2O	Differentiates between (111) and $(\bar{1}\bar{1}\bar{1})$	3
4		1 HNO_3 2 HCl 2 H_2O	Differentiates between (111) and $(\bar{1}\bar{1}\bar{1})$	69

Table A2 continued

TABLE A2 Etches for III-V semiconductors—*continued*

5		1 ml HF 2 ml H_2O 8 mg $AgNO_3$ 1 g CrO_3	Produces dislocation etch pits on (111), $(\bar{1}\bar{1}\bar{1})$, (100) and (110) planes	36
6		1 HNO_3 9 H_2O	Reveals p–n junctions	86
7	GaP	1 HNO_3 2 HCl 2 H_2O	Polishes {111} when used hot	70
8		8 ml HF 10 ml H_2O 40 mg $AgNO_3$ 5 g CrO_3	Used at 75°C. Shows up dislocations and stacking faults on (111) and $(\bar{1}\bar{1}\bar{1})$ surfaces after 15 min. Also delineates p–n junctions	71 89
9		As etch 1	Highest-quality surface obtained from 1% solution, which removes about $\frac{1}{4}$ μm min^{-1}	72
10	GaSb	As etch 1	Polished surface	52
11		2 HNO_3 1 HF 1 CH_3COOH	Polished surface with pits on (111)	34
12		1 H_2O 1 HCl 2 H_2O	Develops etch pits	73
13	InAs	As etch 1	Polishes (111) and $(\bar{1}\bar{1}\bar{1})$ faces	74
14		CP4	See Table A1, etch 5	28
15		Conc. HCl	Gives etching rate of 5 mg cm^{-2} min^{-1} at 75°C	73 75
16		3 HNO_3 1 HF 2 H_2O	Delineates p–n junctions in 1-3 min	74
17	InP	As etch 1	Produces high-quality surface polish using 1% solution	10 52
18		1 HCl 1 HNO_3	For $(\bar{1}\bar{1}\bar{1})$ and (100) surfaces. Produces hillocks on $(\bar{1}\bar{1}\bar{1})$	10
19		As etch 13	Produces etch figures	10
20		0.4N solution of $FeCl_3$ in HCl	Etch pits produced on $(\bar{1}\bar{1}\bar{1})$, (111) and (100) faces	10 34
21	InSb	1 HNO_3 2 HF 1 CH_3COOH	Gives polished surface with pits on (111)	34
22		0.2N solution of $FeCl_3$ in HCl	Develops etch pits	34
23		1 HF 1 H_2O_2 8 H_2O 0.4% *n*-butylthiobutane	Develops β-dislocation etch pits on A and B surfaces	9 76
24		I_2 in CH_3OH	Polishes	52

TABLE A3 Etches for II-VI semiconductors

	Semiconductor	Etchant	Remarks	Reference
1	ZnS	0.5M $K_2Cr_2O_7$ in 16N H_2SO_4	Used for 10 min at 95°C. High polish, with etch pits on (111)	30
2		Conc. HNO_3	2 to 5 min, boiling. Produces etch pits	77
3	ZnSe	0.5% Br_2 in CH_3OH	Soaked in CS_2 for 45 min after etching to remove deposit. Produces etch pits on (111)	55 78
4		3 HNO_3 1 HCl	Produces pits on $(\bar{1}\bar{1}\bar{1})$. Wash in CS_2 after etching, as for etch 3	78
5	ZnTe	3 HNO_3 4 HF	Wash in conc. HCl after etching, to remove film	30
6		2 H_2O_2 3 HF 1 H_2O	Differentiates (111) from $(\bar{1}\bar{1}\bar{1})$	30
7		As etch 3		55
8	CdS	1 ml H_2SO_4 100 ml H_2O 0.08 g Cr_2O_3	Used for 10 min at 80°C. Differentiates between (0001) and $(000\bar{1})$ surfaces	79
9		6 fuming HNO_3 6 CH_3COOH 1 H_2O	Used for 2 min. Sharply defined hexagonal pits on $(000\bar{1})$	30
10		As etch 1	5 to 10 min at 95°C	30
11	CdSe	30 HNO_3 0.1 HCl 20 H_2SO_4 10 CH_3COOH	8 sec at 40°C. A thick film develops, which can be dissolved in conc. H_2SO_4	30
12		1 HNO_3 1 HCl	Pits on (0001)	80
13	CdTe	As etch 6	Polishes (111) and $(\bar{1}\bar{1}\bar{1})$. Etch pits on $(\bar{1}\bar{1}\bar{1})$	30
14		As etch 3		55
15	CdTe	10 ml HNO_3 20 ml H_2O 4 g $K_2Cr_2O_7$	Mirror-like surface	81
16		Etch 14 plus 0.5-10 mg $AgNO_3$	Etch-pit formation	81
17		2 HNO_3 2 HCl 1 H_2O	Polished surface	81
18		10 ml etch 16 10 mg Br_2	Etch pit formation. Develops p–n junctions	81
19	PbS	1 HCl 3 10% thiourea	1-10 min at 60°C. Reveals dislocations	82
20		30 HCl 10 HNO_3 1 CH_3COOH	Etch for a few min at 50°C and then wash in 10% acetic acid	82

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